WHAT IS CLAIMED IS:

1. A method, comprising:

monitoring a number of up and down frequency corrections made by a clock and data recovery phase-lock loop;

for each of a number of time periods, netting together the number of up and down frequency corrections made by the phase-lock loop during the time period; and

deriving one or more operating indications from the net numbers.

2. The method of claim 1, further comprising:

de-serializing the monitored up and down frequency corrections to form parallel words of up and down frequency corrections; and

for each of the number of time periods, performing said netting on the up and down frequency corrections contained within one or more of the parallel words.

3. The method of claim 1, wherein said deriving comprises generating an operating indication if any one of the net numbers is non-zero.

4. The method of claim 3, wherein the operating indication is generated by setting a built-in self-test sticky bit.

5. The method of claim 1, wherein said deriving comprises:

comparing each net number to one or more thresholds; and

if any of the net numbers exceeds one of the thresholds, generating an operating indication.

6. The method of claim 5, wherein the operating indication is generated by setting a built-in self-test sticky bit.

7. The method of claim 5, wherein each of said net numbers is associated with a sign, and wherein the one or more thresholds comprise positive and negative thresholds.

8. The method of claim 1, wherein said deriving comprises:

comparing each net number to a maximum of previously encountered net numbers, and if a net number exceeds the maximum net number, setting the maximum net number to the net number; and

providing the maximum net number as one of the operating indications.

9. The method of claim 1, further comprising, outputting each of the net numbers to built-in self-test hardware.

10. Apparatus, comprising:

an accumulator stage to i) receive up and down frequency corrections

from a clock and data recovery phase-lock loop, and ii) for each of a number of time periods, net together the number of up and down frequency corrections that were received during the time period;

a timer to reset the accumulator at the start of each time period; and

logic to compare each net number to one or more thresholds and provide one or more operating indications based on said comparisons.

11. The apparatus of claim 10, further comprising a de-serializing stage, between the phase-lock loop and the accumulator stage, to output sets of the up and down frequency corrections to the accumulator stage as parallel words of up and down frequency corrections.

12. The apparatus of claim 10, further comprising a capture stage to capture net numbers from the accumulator stage and, at the end of each time period, provide a net number to said logic.

13. The apparatus of claim 12, wherein net numbers stored by the capture stage are dumped to built-in self-test hardware.

14. The apparatus of claim 10, wherein said accumulator stage, timer and logic are clocked by a test clock having a frequency that is lower than that of the phase-lock loop.

15. The apparatus of claim 10, wherein said one or more thresholds is zero, and wherein said logic sets an operating indication if any of the net numbers is non-zero.

16. The apparatus of claim 10, wherein, if a net number exceeds one of said thresholds, said logic provides an operating indication by setting a built-in self-test sticky bit.

17. The apparatus of claim 10, wherein said logic sets a threshold equal to a net number if the net number exceeds the threshold.

18. Apparatus, comprising:

means for monitoring a number of up and down frequency corrections made by a clock and data recovery phase-lock loop;

means to, for each of a number of time periods, net together the number of up and down frequency corrections that were made by the phase-lock loop; and

means to derive one or more operating indications from the net numbers.